QOP 505/515

Network Processor-Based 8-/16-Port QoS Switch with Host CPU

NP Switch (OctaveRG) Features

- ORG800/1600-based network processor (NP) switch
- 7 (QOP505) / 15 (QOP515) half and full-duplex FE ports from NP switch and 1 FE/GbE port from CPU
- 120-byte packet header lookup → all field remarkable
- Address & policy table embedded: up to 4K entries
- Packet buffer embedded
- 4K VLAN support
- IEEE 802.1Q support based on port, MAC, tag, subnet protocol
- Stacked VLAN (Q-in-Q)
- IGMP snooping support: v1, v2, v3
- Filtering against broadcast storm and by L2~L4 fields: filtering rules can be added if necessary
- Link Aggregation function -IEEE 802.3ad
- Management support: SNMP, RMON, SMON
- Flow control (IEEE 802.3x pause function)
- Loop resolution –STP (Spanning Tree Protocol), Rapid STP (802.1W), Per VLAN STP
- IPv6 switch ready due to 120-bytes header lookup

L2/3/4 Performance, NAT/NApT

- Wire-speed Layer 2/3 switching and Layer 4 policy based switching
- Wire-speed NAT/NApT
- Wire-speed session detection and access control

Peripheral Interfaces

- One RGMII/MII interfaces (MAC or PHY mode) for external transceivers
- Embedded USB2.0-compliant host PHY and controller supporting two external USB devices simultaneously
- UART serial channel supporting up to 1.5Mbps
- 8-/16-bit external I/O interface supporting PCMCIA interface or generic DSP/CPU host interfaces
- 21 GPIO pins
- PCI v2.2-compliant host bridge (running up to 66MHz) supports up to three (3) external PCI-based devices

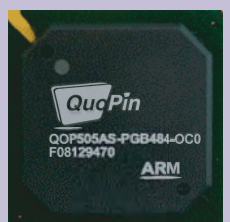
QoS All Features Covered

- ACL (access control list) by L1 ~ L4 (12-tuple) NetBIOS/NetBEUI, mask/range match, unicast/multicast/broadcast/unknown MAC, unicast/multicast IP packet
- ACL Output
  Remarking, VLAN ID insert, filtering, port redirection, port mirroring, CPU redirection, CPU mirroring
- Prioritization
  L2 CoS, L3 IPv4 TOS, L3 IPv4 DSCP, L3 IPv4 IP-precedence packet type (unicast/multicast), IPv6 TC
- Policing
  Granularity, token bucket, priority based multi-stage policing, operation position, port based policing, flow based policing
- Shaping
  Buffering max. size, port based shaping, class based shaping
- Scheduling
  SPQ,WFQ,WRR, DWRR
- Rate control support

Integrated ARM9 as Host CPU besides NP

- ARM922-compatible RISC (with 16kB I-cache, 16kB D-cache, 8kB I-scratchpad, 8kB D-scratchpad) memory and memory management unit (MMU) for high-level RTOS, with programmable CPU core clocks up to 250MHz
- Proprietary advanced system bus architecture achieving superior performance
- Support TRACE32 and/or Multi-ICE JTAG debugging interface
- Built-in intelligent power management for normal and power-saving mode of operations
- Support IRQ/FIQ interrupt modes
- Support little-endian ordering

QOP505



QOP505 Block Diagram