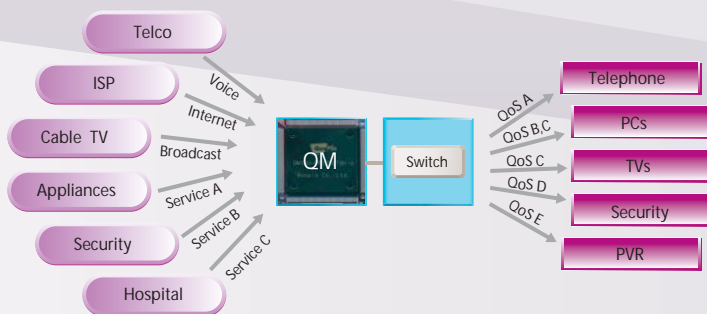# QoS Manager–QM300i

QoS Management Chip Solution

QM series are the first professional QoS management chip solution for value-added QoS services and its management, optimized for access-to-middle edge gateways that must support service-guaranteed quality of services (QoS) for hundreds or thousands of service flows. With the help of embedded packet processor, the QoS manager discerns much bigger number of flows than hardware-fixed ASIC solutions, controls their bandwidth with respect to the services, and regulates flooding flows for each services. Its bandwidth shaping and/or limiting on every flow make such services stable, profitable as entertainment, game, media streaming, and etc.

Specifications

- 3-port x MII
    - One for uplink (WAN), one for downlink (LAN), one for CPU
- 4~2 Priority Queues for a port
    - Priority queues
    - SPQ (Strict priority queue)
    - DWRR (deficit weighted round-robin)
- Thousands of Flows (virtual queues) Support
    - Defined by MAC, IP, Port source/destination addresses or their combination (socket)
- SCE (smart classification engine) Embedded
    - 128-level classification by PHY port, S/D MAC address, Ether type, 802.1p, VID, TOS, Protocol, S/DIP address, TCP/UDP S/D port #
- SGE (subnet grouping engine) Embedded
- Embedded Lookup Table
    - Up-to 4k flows
- IEEE 802.1Q Support: VLAN
    - Based on port, MAC, tag, subnet protocol
- 128Mb SDRAM Packet Buffer (External)
    - Up-to 2K packets
- IEEE 802.3x Pause Function: flow control
- IEEE 802.1p Support: Priority in VLAN tag
- IEEE 802.1x Support: Authentication
- Broadcast Storm Control

Key Features

- Bandwidth measurement for flows
- Virtual Output Queues (VOQ)
    - Thousands of flows are discerned and assigned to queues according to policies.
    - Pass/drop decision for a packet is made by referencing to its designated queue status
- IPC (internal packet control) Network Processor
    - 2048-byte packet processing
    - Insert/delete/translation full support
    - IPv6 tunneling
    - 64~1522-byte packet generation
    - Complete register setting
- Scheduler
    - WAN port: 1k depth, 4 priority queues, SPQ/DWRR, Port BW limit
    - LAN port: 256 depth, 2 priority queues, SPQ/normal, Port BW limit
    - IPC port: 512 depth, 2 priority queues, SPQ/normal, Port BW limit
- Shaping
    - 2-byte escape processing
    - 100Kbps granularity (100Mbps>99.9 Mbps >99.8Mbps …)
- Priority-bit field (802.1p) remarking in a VLAN tag as per:
    - User priority bits of VLAN tag, Ether Type field value, TOS field value of IPv4 header, Flow label field value of IPv6 header, Priority packets assigned to priority queues.
- Direct PPPoE frame setting without reference to the TOS field and Traffic Class field
    - Ether Type field value: 0x8863, 0x8864
- Access Control List (ACL) & Flow-Based Policing
    - Based on MAC address, IP address, TCP/UDP number, and their combination
    - Enhanced by CAM
- NAT/NAPT for thousands of entries

Home/SOHO/SME QoS Gateway
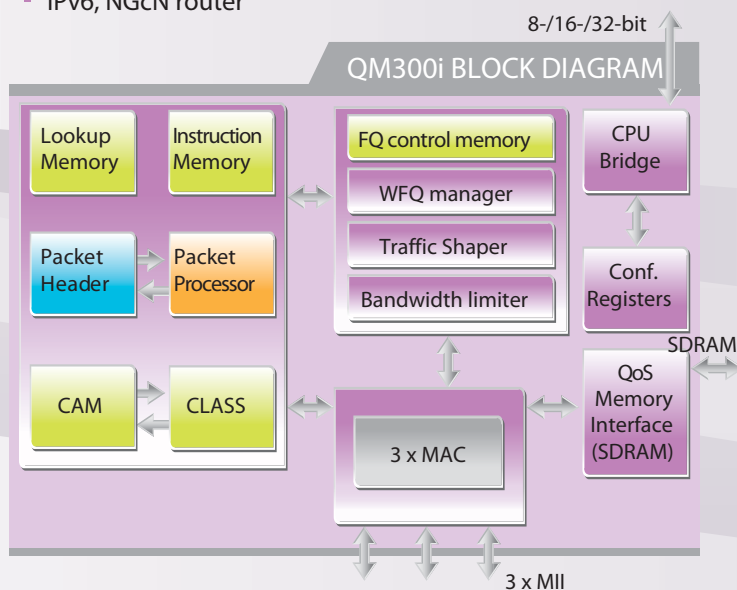

System Architecture
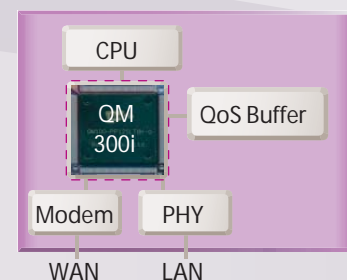
QM300i

QoS Manager Features

Features	QM300i
Access Control	O
Flows	Up-to 4K
Packet Buffer	1,792 packets in total
DiffServ (L3)	O
Bandwidth control	TCP/IP/MAC/Port base
NAT/NApT	O
IPv6 Support	O
MPLS	O (LES)
Interfaces	3 x MII, Local bus
Other Features	Priority remarking DWRR (deficit weighted round-robin) Granularity 0.1Mbps Shaping/Filtering

Applications -Accelerator/Co-Processor

- IP-STB, IP-TV, Residential Gateway
- SOHO router, IP sharer
- AP (access point) for WLAN
- FTTH EPON ONU/ONT
- IPv6, NGcN router

QM300i BLOCK DIAGRAM

8-/16-/32-bit

Lookup Memory | Instruction Memory
Packet Header | Packet Processor
CAM | CLASS

FQ control memory
WFQ manager
Traffic Shaper
Bandwidth limiter

CPU Bridge
Conf. Registers
QoS Memory Interface (SDRAM)

3 x MAC
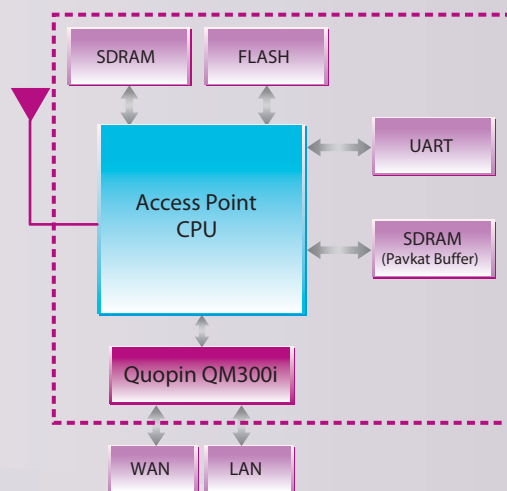
SDRAM

3 x MII

Performance

400Mbps throughput

Access Control

MAC/IP/Port-based access control
Wire-speed flow parsing and filtering

Customization

Customization support for ad-hoc service requirements by means of network processor programming

Enhanced AP System Architecture

SDRAM | FLASH
Access Point CPU
UART
SDRAM (Pavkat Buffer)
Quopin QM300i
WAN | LAN

Interfaces

- 3 x MII: WAN 1-port, LAN 1-port, CPU 1-port
- 8-/16-/32-bit local bus for CPU interface
- External SDRAM for QoS buffers: 64Mb 4 banks

Facts

- Package   289-FGBA
- Power Supply   1.8V Core, 3.3V I/O
- Power Dissipation 1.2 W
- Pcket Processor   200 MHz